



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/603,839	06/26/2000	Keith Barr	05829.0010	3447

22852 7590 09/17/2003

FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER  
LLP  
1300 I STREET, NW  
WASHINGTON, DC 20005

EXAMINER

GANTT, ALAN T

ART UNIT

PAPER NUMBER

2684

DATE MAILED: 09/17/2003

5

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/603,839

Applicant(s)

BARR ET AL.

Examiner

Alan T. Gantt

Art Unit

2684

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 26 June 2000.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-28 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-27 is/are rejected.
- 7) ☒ Claim(s) 28 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 4.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

**DETAILED ACTION**

***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 1 and 24 are rejected under 35 U.S.C. 102(e) as being anticipated by Laor et al.

Regarding claim 1, Laor discloses a data system receiving a periodic data word single as a system single frequency source (figure 2) that is used as a synchronous pipelined switch using serial transmission. The system also uses interface cards, phase locked loops, first and second clock signals. Laor meets the following claim limitations:

- a phase locked loop (PLL) for receiving said WC signal and generating a first clock having a frequency that is a multiple of said WC signal; (Figure 2, clock A,

refs 205 and 206, col. 3, lines 59-67 [signal 206 is a multiple of 10 times the frequency of clock A or system source frequency at the input of the PLL ])

- a clock generator for receiving the first clock and generating a plurality of second clock signals that have frequencies that are submultiples of the first clock signal. (col. 2, lines 29-34; lines col. 4, lines 10-25 [second clock signal is 1/10 the frequency of the first clock, a submultiple])

Regarding claim 24, Laor discloses a data system receiving a periodic data word single as a system single frequency source (figure 2) that is used as a synchronous pipelined switch using serial transmission. The system also uses interface cards, phase locked loops, first and second clock signals. Laor meets the following claim limitations:

- receiving a word clock (WC) signal; (Figure 2, ref. 160)
- generating a first clock having a frequency that is a multiple of said WC signal; (Figure 2, clock A, refs 205 and 206, col. 3, lines 59-67 [signal 206 is a multiple of 10 times the frequency of clock A or system source frequency at the input of the PLL ])
- receiving the first clock and generating a plurality of second clock signals that have frequencies that are submultiples of the first clock signal. (col. 2, lines 29-34; lines col. 4, lines 10-25 [second clock signal is 1/10 the frequency of the first clock, a submultiple])

Art Unit: 2684

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claim 27 is rejected under 35 U.S.C. 102(b) as being anticipated by Campbell.

Regarding claim 27, Campbell discloses a logic gate with controllable hysteresis circuit and high frequency voltage controlled oscillator. The device is on an integrated circuit chip (col. 5, lines 35-46). Additionally, Campbell meets the following limitations:

- a phase comparator (Figure 14, ref. 161);
- a charge pump coupled to an output of the phase comparator; (Figure 14, ref. 172)
- a voltage controlled current source coupled to an output of the charge pump.  
(Figure 14 and col. 9, lines 4-67 [the VCO encompasses the voltage controlled current source])

### *Claim Rejections - 35 USC § 103*

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 2-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Laor, in view of Fujita.

Art Unit: 2684

Regarding claim 2, Laor meets the following limitation:

- the clock generator outputs one of the second clock signals having a same frequency as the WC signal to the PLL, (col. 4, lines 26-36 [clock A is 10 times the input word frequency, clock B is 1/10 of clock A, thus clock B is the same as the input word frequency])

Laor does not use a received second clock to adjust the first clock signal.

Fujita discloses a clock control circuit that teaches and uses a first clock signal inputted to a frequency divider that also includes a multiplication factor that produces a feedback signal (second clock signal) that is input back to the input of the PLL and the frequency/ phase of the two signals is compared to correct the PLL first clock signal. Thus Fujita meets the following limitation:

- said PLL adjusts the first clock signal based on the received one of the second clock signals.(col. 4, lines 14-28 and Figure 1, refs. 5 and 14)

Laor and Fajita are combinable because they share a common endeavor, namely PLL circuits that modify clock frequencies. At the time of the applicant's invention, it would have been obvious to modify Laor to allow an option for correcting the PLL output signal as done by Fajita in order to insure that the desired stability is maintain.

Regarding claim 3, Laor meets the following limitation:

- a control circuit responsive to the second clock signals for generating control signals. (Figure 2, col. 4, lines 41-65 [shift register 232 is clocked at a serial output by a second clock for transmitting serial data to the serial data path])

Regarding claim 4, Laor meets the following limitation:

- a storage element responsive to the control signals for outputting all data words in the storage element. (figure 2, col. 4, lines 41-65 [storage element shift register 232 is clocked at a serial output by a second clock for transmitting serial data to the serial data path])

Regarding claim 5, Laor meets the following limitation:

- a multiplexer for passing the output data to a data pin in response to the control signals. (col. 4, line 66 to col. 5, line 40 [ serial-parallel converter is considered a multiplexer])

Regarding claim 6, Laor meets the following limitations:

- wherein said multiplexer outputs the output data based on a single transition of said WC signal. (col. 4, line 66 to col. 5, line 40 [ serial-parallel converter is considered a multiplexer])

Regarding claim 7, Laor meets the following limitation:

- a storage element responsive to the control signals for receiving data. (figure 2, col. 4, lines 41-65 [shift register 232 is clocked at a serial output by a second clock for transmitting serial data to the serial data path])

Regarding claim 8, Neither Laor nor Fujita meets the following limitations:

- wherein said PLL and clock generator are incorporated on a single chip.

Art Unit: 2684

However, the examiner takes Official Notice that it is well known to incorporate a PLL onto a single integrated circuit chip and at the time of the applicant's invention it would have been obvious to make this modification for the sake of convenience.

Regarding claim 9, Neither Laor nor Fujita meet the following limitations:

- wherein said PLL includes a charge pump.

However, the examiner takes Official Notice that it is well known to incorporate a PLL having a charge pump onto a single integrated circuit chip and at the time of the applicant's invention it would have been obvious to make this modification for the sake of convenience.

7. Claims 10-23, 25, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bowers, in view of Laor et al.

Regarding claim 10, Bowers discloses a serial communication system for two integrated circuit devices having a separate master chip connected to both IC devices with the master chip having a clock generator and circuitry for affecting serial data transmission and control between the master chip and the devices. For purposes of this examination the master chip and one IC device in combination may be considered the transmitter while the other IC is the receiver.

Bowers, as a data system for generating the word clock signal, meets the following limitations:

- A transmitter including a first input for receiving said WC signal, (Figure 5)
- first means for generating a plurality of clock signals based on the WC signal;  
(Figure 4)



Art Unit: 2684

- a first output connected to a transmission line for the transmission of data;  
(Figures 5 and 4)
- a receiver including a first input for receiving said WC signal; a second input, connected to said transmission line, for receiving data transmitted by said transmitter; (Figure 5 [the “Data In” line])

Bowers does not provide for generating a plurality of clock signals based on the word clock.

Laor discloses a data system receiving a periodic data word single as a system single frequency source (figure 2) that is used as a synchronous pipelined switch using serial transmission. The system also uses interface cards, phase locked loops, first and second clock signals. Laor has input ports, which, with the interface, act as receiver and output ports, which, with the interface, act as a transmitter. Since there is a first and second clock generation at the ports and interfaces, Laor meets the following limitation:

- and second means for generating a plurality of clock signals based on the WC signal (Figures 1 and 2 and col. 2, lines 29-34 and col. 3, lines 45-67 and col. 9, lines 22-33).

Bowers and Laor are combinable because they share a common endeavor, namely deices providing for serial data transmission. At the time of the applicant’s invention it would have been obvious to modify Bowers to include a second means for generating a plurality of clock signals based on the work clock signal as done by Laor as this provides for more option due to the versatility of varied clock signaling.

Regarding claim 11, Laor meets the following limitations:

Art Unit: 2684

- wherein the first means for generating includes: a phase locked loop (PLL) for receiving said WC signal and generating a first clock having a frequency that is a multiple of said WC signal; (Figure 2, clock A, refs 205 and 206, col. 3, lines 59-67 [signal 206 is a multiple of 10 times the frequency of clock A or system source frequency at the input of the PLL ])
- a clock generator for receiving the first clock and generating a plurality of second clock signals that have frequencies that are submultiples of the first clock signal. (col. 2, lines 29-34; lines col. 4, lines 10-25 [second clock signal is 1/10 the frequency of the first clock, a submultiple])

Regarding claims 12 and 18, Laor meets the following limitation:

- wherein said clock generator outputs one of the second clock signals having a same frequency as the WC signal to the PLL, ((col. 4, lines 26-36 [clock A is 10 times the input word frequency, clock B is 1/10 of clock A, thus clock B is the same as the input word frequency])

Neither Bowers nor Laor use a received second clock to adjust the first clock signal and do not meet the following limitation:

- said PLL adjusts the first clock signal based on the received one of the second clock signals.

However the examiner takes Official Notice that it is well known to feed back a signal to PLL circuit input to compare with the clock signal and it would have been obvious to modify the

Art Unit: 2684

Bowers / Laor combination to include such a comparison for the purpose of signal preciseness and stability.

Regarding claims 13, 19, and 25, Laor meets the following limitation:

- a control circuit responsive to the second clock signals for generating control signals. (figure 2, col. 4, lines 41-65 [shift register 232 is clocked at a serial output by a second clock for transmitting serial data to the serial data path])

Regarding claim 14, Laor meets the following limitation:

- a storage element responsive to the control signals for outputting all data words in the storage element. (figure 2, col. 4, lines 41-65 [storage element shift register 232 is clocked at a serial output by a second clock for transmitting serial data to the serial data path])

Regarding claims 15, Laor meets the following limitation:

- a multiplexer for passing the output data to a data pin in response to the control signals. (col. 4, line 66 to col. 5, line 40 [serial-parallel converter is considered a multiplexer])

Regarding claims 16 and 26, Laor meets the following limitation:

- wherein said multiplexer outputs the output data based on a single transition of said WC signal. (col. 4, line 66 to col. 5, line 40 [serial-parallel converter is considered a multiplexer])

Art Unit: 2684

Regarding claim 17, Laor meets the following limitations wherein the second means for generating includes:

- a phase locked loop (PLL) for receiving said WC signal and generating a first clock having a frequency that is a multiple of said WC signal; (Figure 2, clock A, refs 205 and 206, col. 3, lines 59-67 [signal 206 is a multiple of 10 times the frequency of clock A or system source frequency at the input of the PLL ])
- a clock generator for receiving the first clock and generating a plurality of second clock signals that have frequencies that are submultiples of the first clock signal. (col. 2, lines 29-34; lines col. 4, lines 10-25 [second clock signal is 1/10 the frequency of the first clock, a submultiple])

Regarding claim 20, Bowers meets the following claim:

wherein said transmitter is incorporated on a single chip ( col. 4, lines 7-23[Bowers uses a single IC chip for each of its slave devices and its master device])

Regarding claim 21, neither Bowers nor Laor meet the following limitation:

- wherein the transmitter includes a phase locked loop (PLL), said PLL having a charge pump.

However, the examiner takes Official Notice that it is well known to incorporate a PLL having a charge pump onto a single integrated circuit chip and at the time of the applicant's invention it would have been obvious to make this modification for the sake of convenience.

Art Unit: 2684

Regarding claim 22, Bowers meets the following claim:

wherein said receiver of claim 21 is incorporated on a single chip. ( col. 4, lines 7-23[Bowers uses a single IC chip for each of its slave devices and its master device])

Regarding claim 23, neither Bowers nor Laor meet the following limitation:

- wherein the receiver includes a phase locked loop (PLL), said PLL having a charge pump.

However, the examiner takes Official Notice that it is well known to incorporate a PLL having a charge pump onto a single integrated circuit chip and at the time of the applicant's invention it would have been obvious to make this modification for the sake of convenience.

#### ***Allowable Subject Matter***

8. Claim 28 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: A phase locked loop circuit with the configuration described was neither found, suggested, nor made evident by the prior art.

#### ***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Art Unit: 2684

Van Steenbrugge discloses a data transfer system that transfers from more than two data words from a transmitter to a receiver in a time-multiplexed manner.

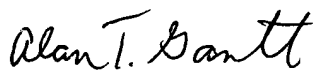
Anderson et al. discloses an extendible-range voltage-controlled oscillator.

Hohmann et al discloses a video dot clock generator that includes a phase-locked loop.

Fisher et al. discloses a digital phase-locked loop with a pulse controlled charge pump.

Any inquiry concerning this communication from the examiner should be addressed to Alan Gantt at telephone number (703) 305-0077. The examiner can normally be reached between 9:30 AM and 6 PM within the Eastern Time Zone. The group FAX number is (703) 308-6306.

Any inquiry of a general nature or relating to this application should be directed to the group receptionist at telephone number (703) 305-4700.

  
Alan T. Gantt



September 4, 2003